IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (original): A solid-state imaging device comprising:

an imaging area having unit cells arranged in a two-dimensional fashion on a semiconductor substrate, each of the unit cells including first and second photoelectric conversion/storage sections for photoelectrically converting incident light and storing charges thus generated, first and second charge readout circuits for transferring charges stored in the first and second photoelectric conversion/storage sections to a common charge detecting section, a potential detecting circuit for detecting charges transferred to the charge detecting section, generating a potential corresponding to an amount of detected charges and transmitting the potential to a corresponding one of vertical signal lines, a reset circuit for discharging the charges transferred to the charge detecting section, and an address circuit for selectively activating the potential detecting circuit;

a vertical driving circuit provided in correspondence to each pixel row of said imaging area, for driving the first and second charge readout circuits, reset circuit and address circuit of each of the unit cells at preset timings;

signal processing circuits respectively attached to the vertical signal lines which are provided for respective columns of the unit cells, for performing required signal processes;

a horizontal driving circuit for scanning outputs of said signal processing circuits in a horizontal direction at preset timings to detect the same; and

an output circuit for outputting output signals of said signal processing circuits detected by the scanning operation by said horizontal driving circuit;

wherein the solid-state imaging device has a first operation mode in which the first and second charge readout circuits are driven at substantially the same timing by said vertical

driving circuit, the charges stored in the first and second photoelectric conversion/storage sections are transferred to and added together in the charge detecting section, and the potential detecting circuit detects the added charges, generates and transmits a potential corresponding to an amount of detected charges to the vertical signal line, and outputs the potential from said output circuit via said signal processing circuits.

Claim 2 (original): The solid-state imaging device according to claim 1, which further comprises a pixel row selection switching section for controlling said vertical driving circuit based on a signal for specifying the first operation mode and a signal for specifying a second operation mode and in which the first and second charge readout circuits are driven by said vertical driving circuit at substantially the same timing in the first operation mode and the first and second charge readout circuits are driven by said vertical driving circuit at different timings in the second operation mode.

Claim 3 (original): The solid-state imaging device according to claim 1, wherein said vertical driving circuit includes a pulse generating section for outputting an address pulse, first and second readout pulses and reset pulse.

Claim 4 (original): The solid-state imaging device according to claim 1, wherein each of said signal processing circuits includes a noise canceller circuit.

Claims 5-9 (canceled)

Claim 10 (original): A readout method of a solid-state imaging device which includes an imaging area having unit cells arranged in a two-dimensional fashion on a semiconductor

substrate, each of the unit cells including first and second photoelectric conversion/storage sections for photoelectrically converting incident light and storing charges thus generated, first and second charge readout circuits for transferring charges stored in the first and second photoelectric conversion/storage sections to a common charge detecting section, a potential detecting circuit for detecting charges transferred to the charge detecting section, generating a potential corresponding to an amount of detected charges and transmitting the potential to a corresponding one of vertical signal lines, a reset circuit for discharging the charges transferred to the charge detecting section, and an address circuit for selectively activating the potential detecting circuit; a vertical driving circuit provided in correspondence to each pixel row of the imaging area, for driving the first and second charge readout circuits, reset circuit and address circuit of each of the unit cells at preset timings; signal processing circuits respectively attached to the vertical signal lines which are respectively provided for columns of the unit cells, for performing required signal processes; a horizontal driving circuit for scanning outputs of the signal processing circuits in a horizontal direction at preset timing to detect the same; and an output circuit for outputting output signals of the signal processing circuits detected by the scanning operation by the horizontal driving circuit; comprising the steps of:

driving the first and second charge readout circuits at substantially the same timing by use of the vertical driving circuit;

transferring the charges stored in the first and second photoelectric conversion/storage sections to the charge detecting section and adding the charges together;

detecting the added charges by use of the potential detecting circuit;

generating a potential corresponding to an amount of the detected charges and transmitting the potential to the vertical signal line; and

outputting the potential from the output circuit via the signal processing circuit.

Claims 11-12 (canceled)